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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/714,943	11/18/2003	Masami Makuuchi	500.43281X00	3730

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EXAMINER	
SHAPIRO, LEONID	

ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 06/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/714,943	MAKUUCHI ET AL.	
	Examiner	Art Unit	
	Leonid Shapiro	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 12-30-05, 11-18-03
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 8,10, 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Seiichi (JP 2002-197899).

As to claim 8, Seiichi teaches a testing method of a semiconductor device having liquid crystal driving circuit including digital functional unit (See Drawing 1, items 11, 17, paragraph 0010) and an analog functional unit (See Drawing 1, items 19-20, paragraphs 0018-0019), said method comprising the steps of:

functionally dividing said digital functional unit and said analog functional unit from each other (See paragraphs 0006-0008);

and

outputting an output of a test result said digital functional unit to outside of said liquid crystal driving circuit through a first terminal provided on said device without via said analog functional unit (See Drawing 1, item 16, paragraph 0010).

As to claim 10, Seiichi teaches digital functional unit and said analog functional unit are controlled independently of each other to perform testing of said digital functional unit and testing of said analog functional unit in an overlapping manner (See paragraphs 0025-0026).

As to claim 12, Seiichi teaches the testing of said digital functional unit includes a display function test, and the testing of said analog functional unit includes a gradation output test (See paragraphs 0015 and 0026).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-6, 9,11,13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Seiichi in view of Matsumoto (US Patent No. 6,339,388 B1).

As to claim 1, Seiichi teaches a semiconductor device including liquid crystal driving circuit, liquid crystal driving circuit comprising a digital functional unit (See Drawing 1, items 11, 17, paragraph 0010) and an analog functional unit (See Drawing 1, items 19-20, paragraphs 0018-0019) and a second terminal for for outputting an output of a test result of said digital functional unit toward outside of said liquid crystal driving circuit without through said analog functional unit (See Drawing 1, item 16, paragraphs 0007, 0015).

Seiichi does not disclose a first terminal for functionally dividing functional digital functional unit and analog functional unit.

Matsumoto teaches a first terminal for functionally dividing functional digital functional unit and analog functional unit (See Fig. 1,items 15-16, Col. 5, Lines 21-28).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate teaching of Matsumoto into Seiichi system in order to test mixed analog/digital circuit (See Col. 2, Lines 27-31 in Matsumoto reference).

As to claim 2, Seiichi teaches a semiconductor device including liquid crystal driving circuit, liquid crystal driving circuit comprising a digital functional unit (See Drawing 1, items 11, 17, paragraph 0010) and an analog functional unit (See Drawing 1, items 19-20, paragraphs 0018-0019) and a second terminal for for outputting an output of a test result of said digital functional unit toward outside of said liquid crystal driving circuit without through said analog functional unit (See Drawing 1, item 16, paragraphs 0007, 0015).

Seiichi does not disclose a third terminal for functionally dividing functional digital functional unit and analog functional unit and fourth terminal for controlling a test of said analog functional unit externally of said liquid crystal driving circuit independently of said digital functional unit.

Matsumoto teaches a third terminal for functionally dividing functional digital functional unit and analog functional unit (See Fig. 1,items 15-16, Col. 5, Lines 21-28) fourth terminal for controlling a test of said analog functional unit externally of said liquid crystal driving circuit independently of said digital functional unit (See Fig. 1, item 15, Col. 5, Lines 10-17).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate teaching of Matsumoto into Seiichi system in order to test mixed analog/digital circuit (See Col. 2, Lines 27-31 in Matsumoto reference).

As to claim 9, Seiichi teaches a testing method of a semiconductor device having liquid crystal driving circuit including digital functional unit (See Drawing 1, items 11, 17, paragraph 0010) and an analog functional unit (See Drawing 1, items 19-20, paragraphs 0018-0019), said method comprising the steps of:

functionally dividing said digital functional unit and said analog functional unit (See paragraphs 0006-0008).

Seiichi does not disclose controlling testing of analog functional unit externally of liquid crystal driving circuit through a second terminal so as to perform the testingof said analog functional unit independently of said digital functional unit.

Matsumoto teaches controlling testing of analog functional unit externally of liquid crystal driving circuit through a second terminal so as to perform the testing of said analog functional unit independently of said digital functional unit (See Fig. 1,item 15, Col. 5, Lines 21-28).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate teaching of Matsumoto into Seiichi system in order to test mixed analog/digital circuit (See Col. 2, Lines 10-17 in Matsumoto reference).

As to claims 3-4, Seiichi teaches digital display controller and said analog functional unit includes display data storage RAM (Drawing 1, item 17), functional unit includes a gradation voltage generating circuit and voltage selecting circuit (Drawing 1,

items 19-20), and said device includes hold means for holding an output said display data storage RAM (Drawing 1, item 21), and Matsumoto teaches to read data held said hold means outside said liquid crystal driving circuit through a data output terminal and sets predetermined data said hold means from outside said liquid crystal driving circuit through said third (first) terminal unit (See Fig. 1,item 15, Col. 5, Lines 21-28).

As to claims 5-6, Seiichi teaches first terminal is used while sharing with a terminal for use during a normal operation (See Drawing 1, item 16).

As to claim 11, Seiichi teaches digital functional unit and said analog functional unit are controlled independently of each other to perform testing of said digital functional unit and testing of said analog functional unit in an overlapping manner (See paragraphs 0025-0026).

As to claim 13, Seiichi teaches the testing of said digital functional unit includes a display function test, and the testing of said analog functional unit includes a gradation output test (See paragraphs 0015 and 0026).

3. Claims 7, 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Seiichi in view of Sakaguchi (US Patent No. 6,766,266 B1).

As to claim 7, Seiichi teaches a semiconductor device having a liquid crystal driving circuit, wherein liquid crystal driving circuit includes a digital functional unit (See Drawing 1, items 11, 17, paragraph 0010) including at least display controller (See Drawing 1, item 12, and an analog functional unit including a gradation voltage

generating circuit and a gradation voltage selecting circuit (See Drawing 1, items 19-20, paragraphs 0018-0019).

Seiichi does not disclose changeover means for changing an output of said gradation voltage generating circuit to a predetermined two-level voltage value.

Sakaguchi teaches changeover means for changing an output of said gradation voltage generating circuit to a predetermined two-level voltage value (See Fig. 5,items 15-17, Col. 8, Lines 35-45).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate teaching of Sakaguchi into Seiichi system in order to reduce the test time (See Col. 2, Lines 55-63 in Sakaguchi reference).

As to claim 14, Seiichi teaches a testing method of a semiconductor device having a liquid crystal driving circuit including a digital functional unit (See Drawing 1, items 11, 17, paragraph 0010) with display controller (See Drawing 1, item 12) and display data storage RAM (See Drawing 1, item 17), and an analog functional unit including a gradation voltage generating circuit and a gradation voltage selecting circuit (See Drawing 1, items 19-20, paragraphs 0018-0019).

Seiichi does not disclose changing an output of said gradation voltage generating circuit to a two-level voltage value by changeover means; selectively setting each gradation voltage at one of different two-level voltage values; and changing an output voltage of said liquid crystal driving circuit two-level voltage to thereby perform a gradation output test.

Sakaguchi teaches changing an output of said gradation voltage generating circuit to a two-level voltage value by changeover means; selectively setting each gradation voltage at one of different two-level voltage values; and changing an output voltage of said liquid crystal driving circuit two-level voltage to thereby perform a gradation output test (See Fig. 5,items 15-17, Col. 8, Lines 35-45).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate teaching of Sakaguchi into Seiichi system in order to reduce the test time (See Col. 2, Lines 55-63 in Sakaguchi reference).

Telephone Inquire

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonid Shapiro whose telephone number is 571-272-7683. The examiner can normally be reached on 8 a.m. to 5 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe can be reached on 571-272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LS
06.08.06

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